**CECS 341 - Lab 5**

**“MIPS Memory Access Stage”**

**Due date: 03/21/19**

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I certify that this submission is my original work

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Lab Report: Lab Assignment 5 - “MIPS Memory Access Stage”

1. **Goal:** The goal of this lab is to understand how the memory stage works in a single cycle MIPS processor. Also there is logic to see if a branch will be taken.
2. **Steps:**
   1. Step 1: Read over the entire lab instructions
   2. Step 2: Copy over the code for the data memory block
   3. Step 3: Copy over the code for the test bench
   4. Step 4: Copy over the skeleton code for the design file
   5. Step 5: Understand how the ALU and signals work for the memory access stage instruction
   6. Step 6: Complete the skeleton code for the design file by filling in the correct inputs and outputs for the module
   7. Step 7: Check each answer with the solution provided and ensure the program is running correctly
3. **Results:** The result of the lab starts off with the data memory location being displayed. Then that memory location displays its contents. That process is repeated 4 times. For example, the last second output has the data memory with its address (dmem[00000000]) which the address is the alu value saved in the aluoute signal. Then that is equal to the contents at that address (= 01010101) which those contents is the value that is saved in the writedatam signal. After that then there is a check to see if the control signals are all working.
4. **Conclusion:** I learned in this lab how to use the Memory Access instruction in the ALU and how the signals work to control it. The challenge of this lab was understanding how the signals and registers were effected by the instruction.